LPDDR3

**4.11.3 Mode Register Write - CA Training Mode**

Because CA inputs operate as double data rate, it may be difficult for memory controller to satisfy CA input setup/hold timings at higher frequency. A CA Training mechanism is provided.

**4.11.3.1 CA Training Sequence**

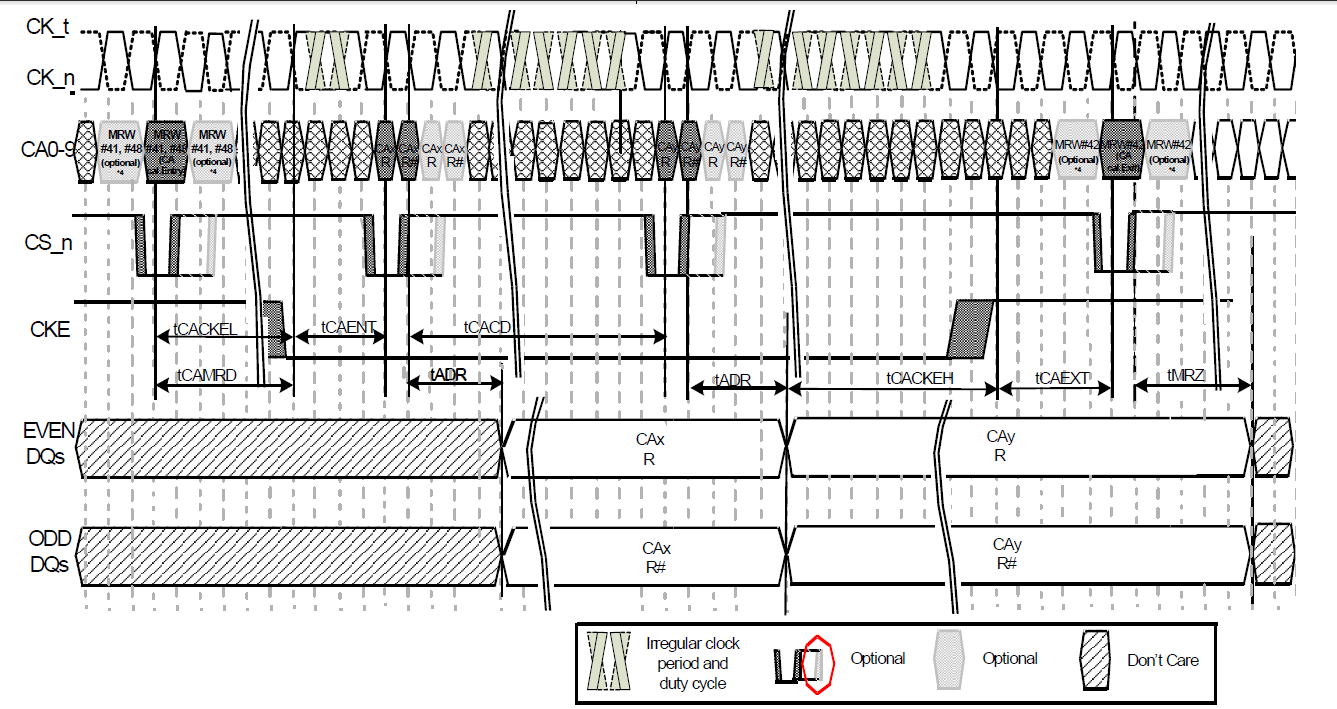
a) CA Training mode entry: Mode Register Write to MR41

b) CA Training session: Calibrate CA0, CA1, CA2, CA3, CA5, CA6, CA7 and CA8 (see !!! Table 19 on page 67)

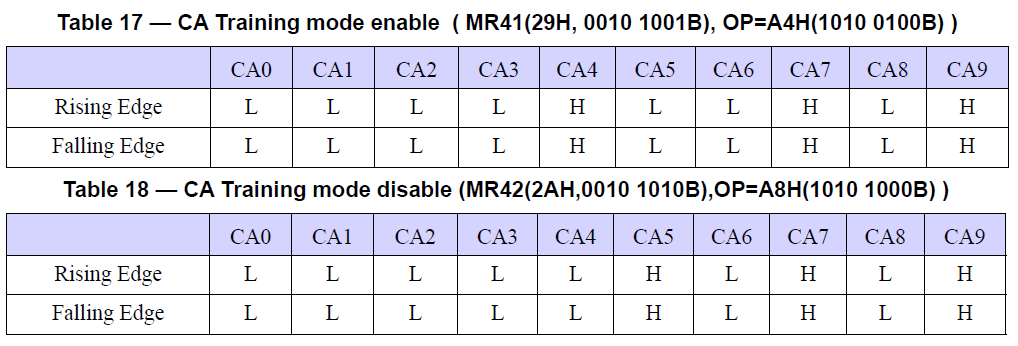
c) CA to DQ mapping change: Mode Register Write to MR48

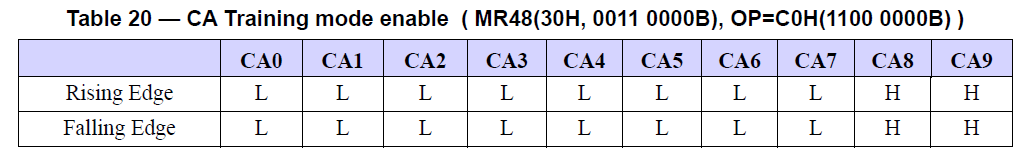
d) Additional CA Training session: Calibrate remaining CA pins (CA4 and CA9) (see !!! Table 21 on page 67)

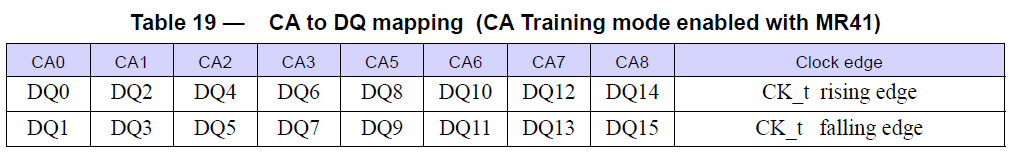
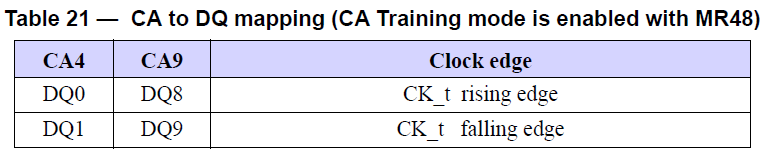
e) CA Training mode exit: Mode Register Write to MR42



我理解d和e之间，还有CAxR和CAxR#的信号需DDR controller去拉。过程应该是先set CA delay，set CAxR和CAxR#，read from DQ(EVEN 偶数，ODD 奇数)，反复这个过程，最终找到CA delay的Windows，取中间值。



 MR41、MR42和MR48上升沿和下降沿，CA线上不变，所以，不管CA delay是多少，DRAM都可以收到这个Command。

上升沿都是偶数的DQ线，下降沿都是奇数的DQ线。共用到16根DQ线。

LPDDR4